WHAT IS CLAIMED IS:

1. A memory array comprising a plurality of memory cells arranged in one or more rows and columns, wherein each memory cell shares at least one contact structure with a vertically adjacent memory cell, wherein the shared contact structure is formed proximate to a boundary between the memory cell and the vertically adjacent memory cell, such that the shared contact structure is formed: i) completely within the memory cell on one side of the boundary, ii) completely within the second memory cell on an opposite side of the boundary, or iii) formed at the boundary, such that unequal portions of the shared contact structure are formed on either side of the boundary.

2. The memory array as recited in claim 1, wherein the shared contact structure is configured for coupling an overlying bit line to an underlying diffusion region.

3. The memory array as recited in claim 1, wherein the shared contact structure is configured for coupling an overlying ground supply line to an underlying diffusion region.

4. The memory array as recited in claim 1, wherein the shared contact structure is configured for coupling an overlying power supply line to an underlying diffusion region.

5. The memory array as recited in claim 1, wherein a length of the memory array is reduced by sharing the contact structure between the memory cell and the vertically adjacent memory cell.

6. The memory array as recited in claim 1, wherein a column of memory cells is formed by rotating vertically adjacent memory cells about an x-axis and a y-axis, wherein the x- and y-axes extend horizontally and vertically, respectively, through a center of each memory cell.

7. The memory array as recited in claim 6, wherein multiple rows of memory cells are formed by replicating the column of memory cells at a location horizontally adjacent to the column.

8. The memory array as recited in claim 7, wherein the column of memory cells comprises a pair of n-type diffusion regions, each formed as a continuous line of constant width and periodically interspersed with rectangular shaped isolation regions.

9. The memory array as recited in claim 8, wherein a complexity of the memory array is minimized by forming the pair of n-type diffusion regions as a continuous line of constant width.

10. The memory array as recited in claim 8, wherein each memory cell in the column comprises a first local word line and a portion of a second local word line, each of which extends only partially across each memory cell.

11. The memory array as recited in claim 10, wherein a distal end of the first local word line is horizontally and vertically spaced from a distal end of the portion of the second local word line over one of the rectangular shaped isolation regions.

12. The memory array as recited in claim 11, wherein a width of the memory array is reduced by horizontally spacing the distal end of the first local word line from the distal end of the portion of the second local word line.

13. The memory array as recited in claim 12, wherein each memory cell in the column comprises two access transistors, which share the first local word line, and an additional access transistor that shares the portion of the second local word line with an access transistor in an adjacent memory cell.

14. The memory array as recited in claim 13, wherein a width of the memory array is reduced by sharing the portion of the second local word line with the adjacent memory cell.

15. The memory device as recited in claim 14, wherein an aspect ratio of the memory device ranges between about 0.3 and about 0.7.

16. A dual-port memory cell, comprising:

a first pair of N-channel access transistors coupled through respective gate terminals by a first local word line of the memory cell;

a second pair of N-channel access transistors coupled through respective gate terminals by separate portions of a second local word line of the memory cell; and

a plurality of bitline contact structures coupled to drain terminals of the first and second pairs of access transistors and to drain terminals of corresponding pairs of access transistors arranged within a vertically adjacent memory cell, wherein the bitline contact structures are formed i) completely within the memory cell, ii) completely within the adjacent memory cell, or iii) having unequal portions within the memory cell and the adjacent memory cell.

17. The dual-port memory cell as recited in claim 16, further comprising first and second inverter circuits, each including a P-channel latch transistor coupled in common-gate configuration with an N-channel latch transistor, wherein drain terminals of the P-channel and N-channel latch transistors are coupled to respective source terminals of the first and second pairs of N-channel access transistors.

18. The dual-port memory cell as recited in claim 17, further comprising a pair of power supply contact structures coupled to source terminals of the P-channel latch transistors and a pair of ground supply contact structures coupled to source terminals of the N-channel latch transistors, wherein the pairs of power and ground supply contact structures are shared between the memory cell and the adjacent memory cell, such that one power supply contact structure and one ground supply contact structure are arranged within each of the memory cells.

19. The dual-port memory cell as recited in claim 18, wherein the access transistors and the latch transistors are formed, such that source/drain current flows through the access and latch transistors along a length of the memory cell.

20. The dual-port memory cell as recited in claim 18, further comprising a first metal layer dielectrically spaced above and coupled to the access transistors and the latch transistors through corresponding contact structures.

21. The dual-port memory cell as recited in claim 20, further comprising a second metal layer dielectrically spaced above and coupled to the first metal layer through a plurality of vias, wherein the second metal layer comprises:

a first pair of complementary bit lines directed along the length of the memory cell and corresponding to a first port;

a second pair of complementary bit lines directed along the length of the memory cell and corresponding to a second port; and

a pair of ground supply lines each directed along the length of the memory cell and arranged between bit lines of dissimilar ports.

22. The dual-port memory cell as recited in claim 21, wherein the dual-port memory cell comprises no other bit lines other than the first and second pair of complementary bit lines.

23. The dual-port memory cell as recited in claim 21, wherein the pair of ground supply lines are configured to provide horizontal capacitive shielding between the bit lines of dissimilar ports.

24. The dual-port memory cell as recited in claim 21, further comprising a third metal layer dielectrically spaced above and coupled to the second metal layer through another plurality of vias, wherein the third metal layer comprises:

a first word line directed along a width of the memory cell and corresponding to the first port;

a second word line directed along the width of the memory cell and corresponding to the second port; and

a ground supply line directed along the width of the memory cell and arranged between the first and second word lines.

25. The dual-port memory cell as recited in claim 24, wherein the ground supply line within the third metal layer is configured to provide horizontal capacitive shielding between the first and second word lines.

26. The dual-port memory cell as recited in claim 24, wherein the ground supply line within the third metal layer is coupled to the pair of ground supply lines within the second metal layer to form a two-dimensional ground supply grid.

27. The dual-port memory cell as recited in claim 24, wherein the third metal layer further comprises a power supply line directed along the width of the memory cell, such that portions of the power supply line are shared between the memory cell and the adjacent memory cell.

28. The dual-port memory cell as recited in claim 27, wherein the first and second word lines, the power supply line and the ground supply line are configured to provide vertical capacitive shielding between the first and second bit lines and a fourth metal layer dielectrically spaced above and coupled to the third metal layer.

29. A system embedded within and/or arranged upon a single substrate, wherein the system comprises:

a memory array comprising a plurality of memory cells, each of which comprises:

a substrate layer comprising four access transistors, two inverter circuits, and a plurality of contact structures formed offset from a boundary between vertically adjacent memory cells sharing the plurality of contact structures;

a second metal layer arranged above the substrate layer and comprising a plurality of bitlines and one or more ground supply lines arranged between and parallel to bitlines of dissimilar ports; and

a third metal layer arranged above the second metal layer and comprising a pair of wordlines and an additional ground supply line arranged between and parallel to wordlines of dissimilar ports, wherein the wordlines and the additional ground supply line are directed perpendicular to the plurality of bit lines; and

one or more subsystems coupled to the memory array through a fourth metal layer arranged above the third metal layer, wherein the fourth metal layer comprises a plurality of transmission lines.

30. The system as recited in claim 29, wherein the third metal layer is configured to vertically shield the second metal layer from stray capacitances from the fourth metal layer.